

A Single Phase 15 Level Inverter Using Single DC Source for Voltage Sag Compensation

T.Kamalkumar¹, S.Manikandan², S.Sunil Kumar³, J.Lakshmanan⁴

U.G Students, Department of EEE, TJS Engineering College, Chennai, Tamil Nadu, India ^{1,2,3},

Assistant Professor, Department of EEE, TJS Engineering College, Chennai, Tamil Nadu, India ⁴

ABSTRACT: The multilevel voltage source inverters unique structure allows them to reach high voltages with low harmonics without use of transformers or series connected synchronized switching devices. The general function of the multilevel inverter is to synthesize a desired voltage from several levels of dc voltages. For this reason multilevel inverters can easily provide the high power required of a large electric drive. As the number increases the synchronized output waveform has more steps, which produces a staircase waveform that approaches a desired waveform. Also as more steps are added to the waveform the harmonic distortion of the output wave decreases approaching zero as the number of levels increases. As the number of levels increases, the voltage that can be spanned summing multiple inverters much that no voltage sharing problems are encountered by the active devices

KEYWORDS: SAG, power factor comparator, influence of renewable energy, dc motor drive.

I. INTRODUCTION

In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium voltage network. Today it is hard to connect a single semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage level. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of switches permit the addition of capacitor voltages, which results as high voltage at output, while the power semiconductor must withstand only reduced voltage. Design for the heavy duty electric and hybrid electric drives will require advanced power electronic inverters to meet the high power demands required of them. Development of large electric drive trains for these vehicles will result in increased fuel efficiency, lower emission, and likely better vehicle performance. Transformer less multilevel inverters is uniquely suited for this application because of the high volt-ampere ratings possible with these inverters. For EVs a cascaded H-bridges inverter can be used to drive the traction motor from a set of batteries or fuel cells. Where generated ac voltage is available such as from an alternator or generator a back-to-back diode clamped converter can convert this source to variable frequency ac voltage for the driven motor. Multilevel inverters also solve problems with some present two level pulse width modulation (PWM) adjustable speed drives (ASD). ASDs usually employ a front end diode rectifier to convert utility ac voltage to dc voltage and an inverter with PWM controlled switching devices to convert the dc voltage to variable frequency and variable voltage of the motor speed control. Motor damage and failure have been reported by industries as a result of some ASD inverters HIGH VOLTAGE CHANGE RATINGS (dv/dt), which produced a common mode voltage across the motor windings. The main problems reported have been "motor bearing failure" and "motor winding insulation breakdown" because of circulating currents, dielectric stress, voltage surge, and converter discharge. Only recently have motor insulation failures become a problem with some ASDs because the increased switching speed of contemporary power semiconductor devices caused steep voltage waveforms to appear at the motor

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 7, Special Issue 2, March 2018

terminals. The voltage change rate (dv/dt) sometimes can be high enough to induce corona discharge between the winding layers. These high-speed semiconductor switches allow faster PWM carrier frequencies. Although the high frequency switching can increase the motor running efficiency and is well above the acoustic noise level, the dv/dt associated dielectric stresses between insulated winding turns also greatly increased. Multilevel inverters overcome these problems because the individual devices have a much lower dv/dt per switching and they operate at high efficiency because they can switch at a much lower frequency than PWM-controlled inverters. The multilevel voltage source inverters unique structure allows them to reach high voltages with low harmonics with out use of transformers or series connected synchronized switching devices. The general function of the multilevel inverter is to synthesize a desired voltage from several levels of dc voltages. for this reason multilevel inverters can easily provide the high power required of a large electric drives As the number increases the synchronized output waveform has more steps, which produces a staircase waveform that approaches a desired waveform. Also as more steps are added to the waveform the harmonic distortion of the output wave decreases approaching zero as the number of levels increases. As the number of levels increases, the voltage that can be spanned summing multiple inverters much that no voltage sharing problems are encountered by the active devices. Using multilevel inverters as drives for electric motors is a much different application than for the utility applications. Only reactive power flows between the converter and the system in staticvar compensation, whereas the converter must handle bi-directional real power flow in the case of motor drives.

II. LITERATURE REVIEW

In 2016 Mohamed Trabelsi This paper presents a multi-objective Model Predictive Control (MPC) for grid-tied 4-cell 15-level Packed U Cells (PUC) inverter. This challenging topology is characterized by high power quality with reduced number of components compared to conventional multilevel inverters. Compared to traditional PI controller, MPC is attracting more interest due to its good dynamic response and high accuracy of reference tracking, through the minimization of a flexible user-defined cost function. For the presented PUC topology, the grid current should be jointly controlled with the capacitors' voltages for ensuring proper operation of the inverter, which leads to an additional requirement of pre-charge circuits for the capacitors in case of using PI current controller (or using additional PI controllers).

In 2013 Zainal Salam; Abdul Moeed Amjad; Ahmed Majed Harmonic elimination pulse width modulation (HEPWM) method has been widely applied to remove harmonics due to its superior frequency spectra. It requires the solution of a set of transcendental nonlinear equations. Soft computing (SC) methods are extensively employed to solve this problem because of their effective global search ability. Differential evolution (DE) has surpassed most of the SC methods in diverse fields but it has never been utilized to solve this problem. In this work, DE is utilized to solve the HEPWM problem for five level cascaded multilevel voltage source inverter (MVSI). Simulation results have shown that the discontinuities of the HEPWM angle trajectories are nullified and a wider over-modulation range has been covered, enhancing the utilization of DC link voltages and extending the application of HEPWM for high power applications.

In 2014 Gaetano Patti; Giuliana Alderisi; Lucia Lo Bello The Low Latency Deterministic Network (LLDN) protocol is defined in the IEEE 802.15.4e, which is an amendment to the IEEE 802.15.4 standard specifically devised to support the requirements of industrial applications. The LLDN provides a TDMA-based medium access mechanism in which the network cycle time grows linearly with the number of nodes. As a result, to offer low cycle times to applications requiring a high number of nodes, the LLDN specifications suggest to create multiple networks operating on different channels by embedding multiple transceivers in the coordinator. However, such an approach entails high costs and increases the design complexity. Moreover, the LLDN protocol foresees a star topology that limits the network area coverage. This paper proposes a novel approach, called a MultiChannel LLDN, based on a hierarchical network structure in which nodes communicate on different channels at the same time.

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

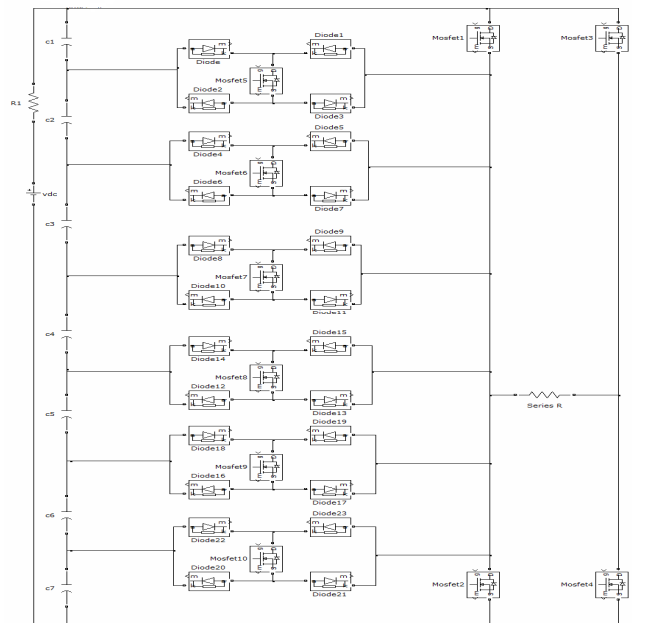
Visit: www.ijirset.com

Vol. 7, Special Issue 2, March 2018

III. PROPOSED SYSTEM

The different topologies presented in the literature as a multilevel inverter show a number of characteristics in common. The main disadvantage associated with the multilevel inverter configuration is their circuit complexity, requiring a high number of power switches. When we are entering the simplified H-Bridge multilevel inverter, power devices will be reduction and circuit complexity also reduction so circuit losses also reducing. Even taking into account the technological tendency to lower the price at which multilevel inverter can compete with standard configuration. As contribution to solve this twin Problem (cumbersome power stage and complex firing control circuit) this work proposes a new converter topology, presented as a block diagram in drastically reducing the power circuit complexity, and a modulator and firing control circuit developed using a controller these two Concepts used in the design of the seven level bridge converters presented below. The new converter topology used in the power stage offers an important improvement in term of lower component count and reduced layout complexity, when compared with the nine level converters presented in the literature. The simplified H-bridge multilevel inverter achieves a reduction in the number of main switch required and uses no more diodes and capacitors that the second best topology, the asymmetric cascade configuration. In the modulator circuit, the FPGA can perform all required modulation functions providing another important reduction in cost and circuit complexity.

IV. PROPOSED SYSTEM CRCUIT DIAGRAM



A. MOSFET (IRF 840)

The layout refinements introduced greatly improve the $R_{on} \cdot \text{area}$ figure of merit while keeping the device at the leading edge for what concerns switching speed, gate. The cross section of a VDMOS (see figure 1) shows the "verticality" of the device: it can be seen that the source electrode is placed over the drain, resulting in a current mainly vertical when the transistor is in the on-state. The diffusion in VDMOS refers to the manufacturing process: the P wells (see figure 1) are obtained by a diffusion process (actually a double diffusion process to get the P and N^+ regions, hence the name double diffused).

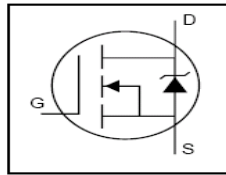
International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 7, Special Issue 2, March 2018

SYMBOL FOR POWER MOSFET



B.BUFFER (74IS244)

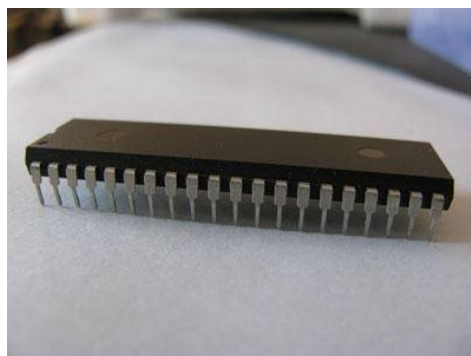
A voltage buffer amplifier is used to transfer a voltage from a first circuit, having a high output impedance level. Op-amps have a variety of uses. One use is as a so-called *buffer*.that *isolates* or *separates* one circuit from another. In order to explain this more precisely, let's take a closer look at our 3-bit DACo a second circuit with a low input impedance level.

C.OPTO ISOLATOR (HTC2E)

There are many situations where signals and data need to be transferred from one subsystem to another within a piece of electronics equipment, or from one piece of equipment to another, without making a direct 'ohmic' electrical connection. Often this is because the source and destination are (or may be at times) at very different voltage levels, like a microprocessor which is operating from 5V DC but being used to control a triac which is switching 240V AC.facts. In such situations the link between the two must be an isolated one, to protect the microprocessor from overvoltage damage.Relays can of course provide this kind of isolation, but even small relays tend to be fairly bulky compared with ICs and many of today's other miniature are also not as reliable and only capable of relatively low speed operation. Where small size, higher speed and greater reliability are important, a much better alternative is to use an optocoupler. These use a beam of light to transmit the

D.MICROCONTROLLER (PIC)

Microcontroller PIC16F877A is one of the PICMicro Family microcontroller which is popular at this moment, start from beginner until all professionals. Because very easy using PIC16F877A and use FLASH memory technology so that can be write-erase until thousand times. The superiority this Risc Microcontroller compared to with other microcontroller 8-bit especially at a speed of and his code compression. PIC16F877A have 40 pin by 33 path of I/O. PIC16F877A perfectly fits many uses, from automotive industries and controlling home appliances to industrial instruments, remote sensors, electrical door locks and safety device .It is also ideal for smart cards as well as for battery supplied devices because of its low consumption. EEPROM memory makes it easier to apply microcontrollers to devices where permanent storage of various parameters is needed (codes for transmitters, motor speed, receiver frequencies, etc.). Low cost, low consumption, easy handling and flexibility make PIC16F877A applicable even in areas where microcontrollers had not previously been considered (example: timer functions, interface replacement in larger systems, coprocessor applications, In System Programmability of this chip (along with using only two pins in data transfer) makes possible the flexibility of a product, after assembling and testing have been completed. This capability can



PIC MICROCONOLLER

E.RECTIFIER UNIT

In the power supply unit, rectification is normally achieved using a solid state diode. Diode has the property that will let the electron flow easily in one direction at proper biasing condition . As AC is applied to the diode, electrons only flow

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 7, Special Issue 2, March 2018

when the anode and cathode is negative. Reversing the polarity of voltage will not permit electron flow. During the positive half cycle. The DC voltage appearing across the output terminals of the bridge rectifier will be somewhat less than 90% of the applied rms value. Normally one alteration of the input voltage will reverse the polarities.



Fig:3 Hardware Snapshot Of A SINGLE PHASE 15 LEVEL
INVERTER USING SINGLE DC SOURCE FOR VOLTAGE SAG
COMPENSATION

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 7, Special Issue 2, March 2018

V. CONCLUSION

A multilevel inverter with individual dc sources has been posed for use in large electric drives. Simulation and experimental results have shown that with a control strategy operates the switches at the fundamental frequency, these converters have low output voltage THD and high efficiency and power factor.

In summary the main advantages of using multilevel converters for large electric drives include the following,

1. They are suitable for large volt-ampere rated and/or high voltage motor drives.
2. These multilevel converters systems have higher efficiency because the devices can be switched at minimum frequency.
3. Power factor is close to unity for multilevel inverters used as a rectifier to convert generated ac to dc.
4. No EMI problem or common mode voltage/current problem exists.
5. No charge unbalance problem results when the converters are in higher charge mode or drive

REFERENCES

- [1] J. V. Milanovic and Y. Zhang, "Global minimization of financial losses due to voltage sags with facts based devices," IEEE Transactions on Power Delivery, vol. 25, no. 1, pp. 298–306, Jan. 2010.
- [2] J. A. Martinez and J. Martin-Arnedo, "Voltage sag studies in distribution networks-part i: system modeling," IEEE Transactions on Power Delivery, vol. 21, no. 3, pp. 1670–1678, Jul. 2006.
- [3] P. Kanjiya, B. Singh, A. Chandra, and K. Al-Haddad, "Srf theory revisited to control self-supported dynamic voltage restorer (dvr) for unbalanced and nonlinear loads," IEEE Transactions on Industry Applications, vol. 49, no. 5, pp. 2330–2340, Sep. 2013.
- [4] A. O. Ibrahim, T. H. Nguyen, D. C. Lee, and S. C. Kim, "A fault ride-through technique of dfig wind turbine systems using dynamic voltage restorer," IEEE Transactions on Energy Conversion, vol. 26, no. 3, pp. 871–882, Sep. 2011.
- [5] Y. W. Li, D. M. Vilathgamuwa, P. C. Loh, and F. Blaabjerg, "A dualfunctional medium voltage level dvr to limit downstream fault currents," IEEE Transactions on Power Electronics, vol. 22, no. 4, pp. 1330–1340, Jul. 2007.
- [6] Y. W. Li, D. M. Vilathgamuwa, F. Blaabjerg, and P. C. Loh, "A robust control scheme for medium-voltage-level dvr implementation," IEEE Transactions on Industrial Electronics, vol. 54, no. 4, pp. 2249–2261, Aug. 2007.
- [7] M. Radmehr, S. Farhangi, and A. Nasiri, "The power of paper – effects of power quality distortions on electrical drives and transformer life in paper industries," IEEE Industry Applications Magazine, vol. 13, no. 5, pp. 38–48, Sep. 2007.
- [8] A. M. Rauf and V. Khadkikar, "An enhanced voltage sag compensation scheme for dynamic voltage restorer," IEEE Transactions on Industrial Electronics, vol. 62, no. 5, pp. 2683–2692, May. 2015.
- [9] F. B. Ajaei, S. Afsharnia, A. Kahrobaei, and S. Farhangi, "A fast and effective control scheme for the dynamic voltage restorer," IEEE Transactions on Power Delivery, vol. 26, no. 4, pp. 2398–2406, Oct. 2011.
- [10] D. M. Vilathgamuwa, A. A. D. R. Perera, and S. S. Choi, "Voltage sag compensation with energy optimized dynamic voltage restorer," IEEE Transactions on Power Delivery, vol. 18, no. 3, pp. 928–936, Jul. 2003.
- [11] S. S. Choi, J. D. Li, and D. M. Vilathgamuwa, "A generalized voltage compensation strategy for mitigating the impacts of voltage sags/swells," IEEE Transactions on Power Delivery, vol. 20, no. 3, pp. 2289–2297, Jul. 2005.
- [12] Q. Wang and S. S. Choi, "An energy-saving series compensation strategy subject to injected voltage and input-power limits," IEEE Transactions on Power Delivery, vol. 23, no. 2, pp. 1121–1131, Apr. 2008.
- [13] C. Meyer, R. W. D. Doncker, Y. W. Li, and F. Blaabjerg, "Optimized control strategy for a medium-voltage dvr-2014; theoretical investigations and experimental results," IEEE Transactions on Power Electronics, vol. 23, no. 6, pp. 2746–2754, Nov. 2008.
- [14] A. K. Sadigh and K. M. Smedley, "Review of voltage compensation methods in dynamic voltage restorer (dvr)," in 2012 IEEE Power and Energy Society General Meeting, Jul. 2012, pp. 1–8.
- [15] P. Roncero-Sanchez, E. Acha, J. E. Ortega-Calderon, V. Feliu, and A. Garcia-Cerrada, "A versatile control scheme for a dynamic voltage restorer for power-quality improvement," IEEE Transactions on Power Delivery, vol. 24, no. 1, pp. 277–284, Jan. 2009.
- [16] H. K. Al-Hadidi, A. M. Gole, and D. A. Jacobson, "Minimum power operation of cascade inverter-based dynamic voltage restorer," IEEE Transactions on Power Delivery, vol. 23, no. 2, pp. 889–898, Apr. 2008.
- [17] H. K. Al-Hadidi, A. M. Gole, and D. A. Jacobson, "A novel configuration for a cascade inverter-based dynamic voltage restorer with reduced energy storage requirements," IEEE Transactions on Power Delivery, vol. 23, no. 2, pp. 881–888, Apr. 2008.
- [18] P. Jayaprakash, B. Singh, D. P. Kothari, A. Chandra, and K. Al-Haddad, "Control of reduced-rating dynamic voltage restorer with a battery energy storage system," IEEE Transactions on Industry Applications, vol. 50, no. 2, pp. 1295–1303, Mar. 2014.
- [19] D. M. Vilathgamuwa, P. C. Loh, and Y. Li, "Protection of microgrids during utility voltage sags," IEEE Transactions on Industrial Electronics, vol. 53, no. 5, pp. 1427–1436, Oct. 2006.